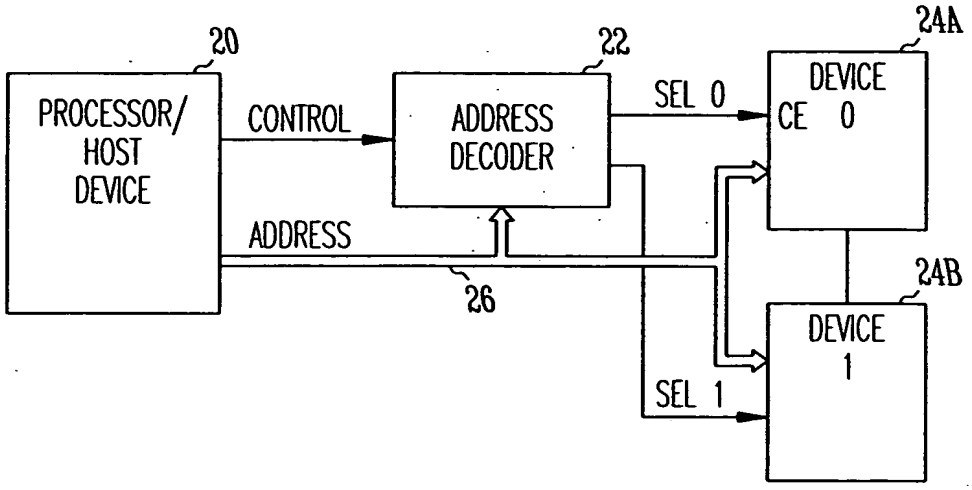


Fig.1 (Prior Art)

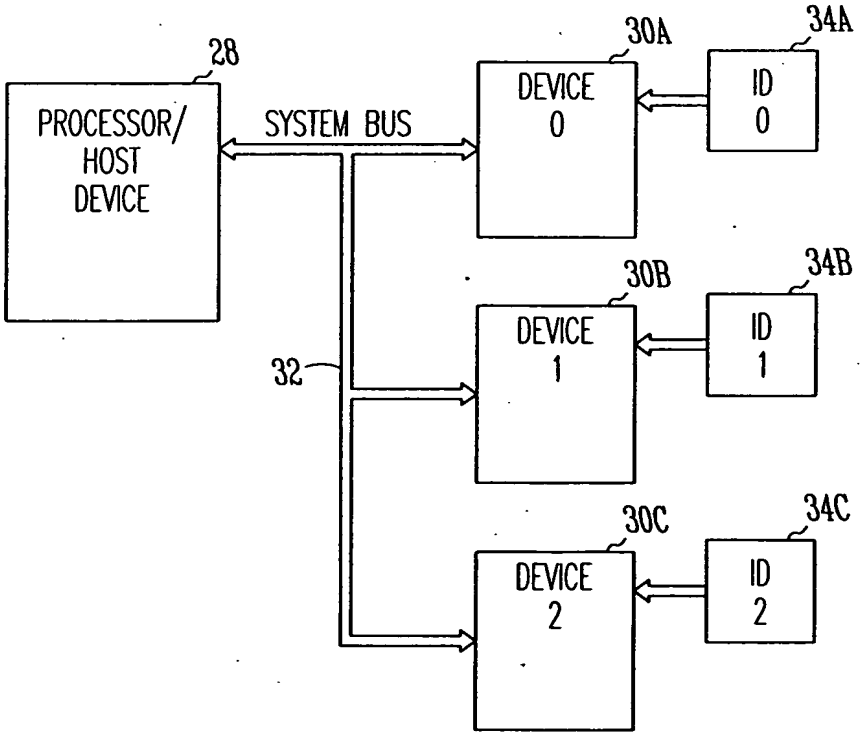


Fig.2 (Prior Art)

SCANNED BY SIGNATURE

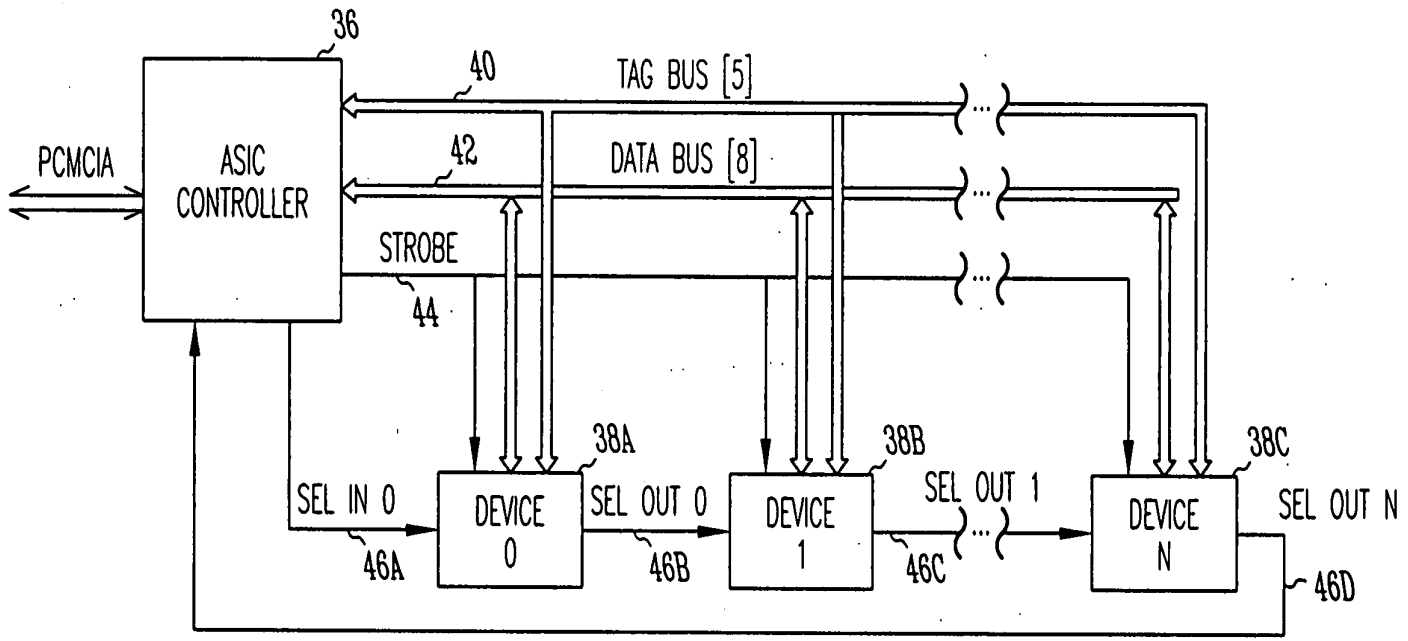


Fig. 3A

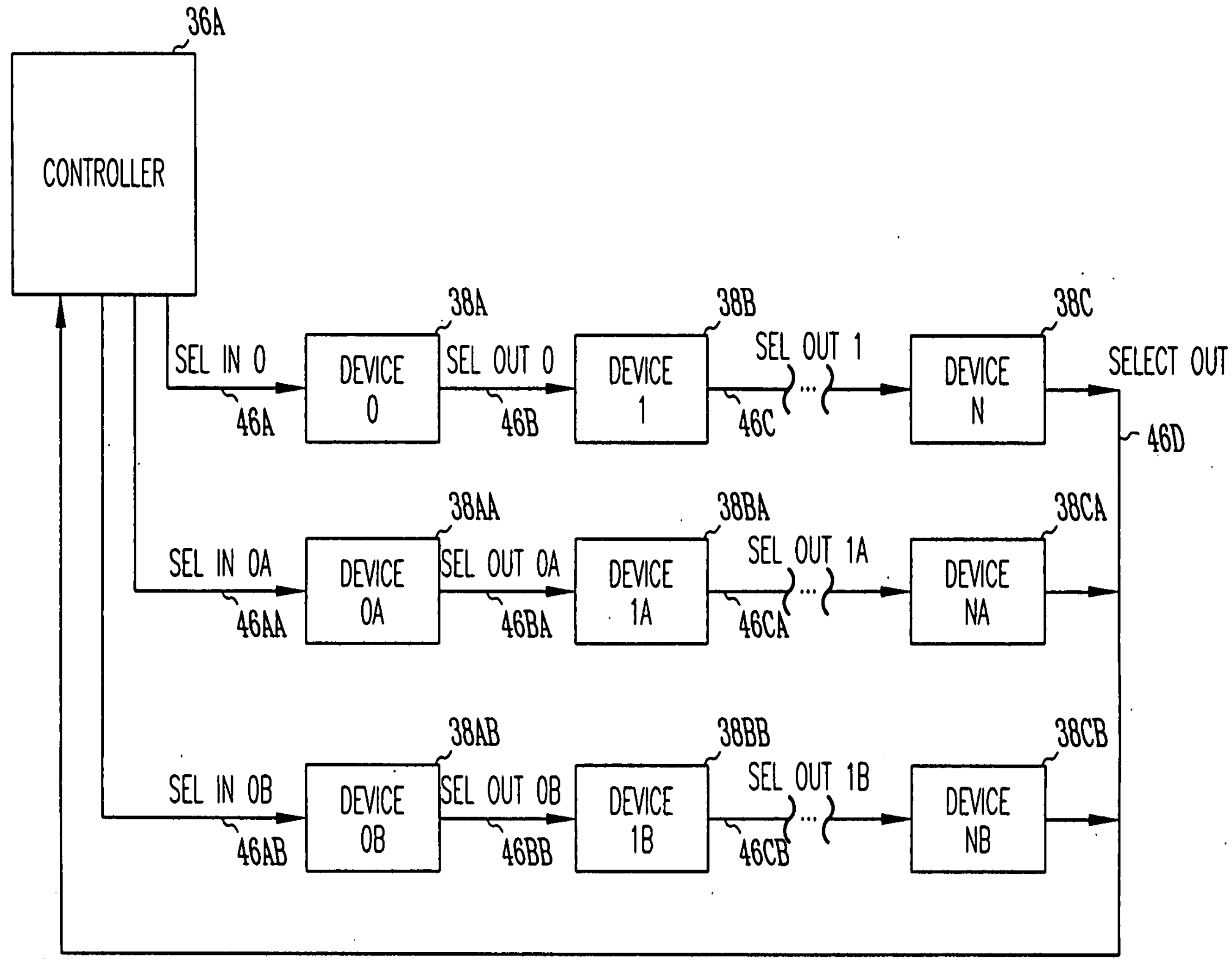

36A
CONTROLLER
SEL IN 0
46A
38A
DEVICE 0
SEL OUT 0
46B
38B
DEVICE 1
SEL OUT 1
46C
38C
DEVICE N
SELECT OUT
46D
SEL IN 0A
46AA
38AA
DEVICE 0A
SEL OUT 0A
46BA
38BA
DEVICE 1A
SEL OUT 1A
46CA
38CA
DEVICE NA
SEL IN 0B
46AB
38AB
DEVICE 0B
SEL OUT 0B
46BB
38BB
DEVICE 1B
SEL OUT 1B
46CB
38CB
DEVICE NB

Fig.3B

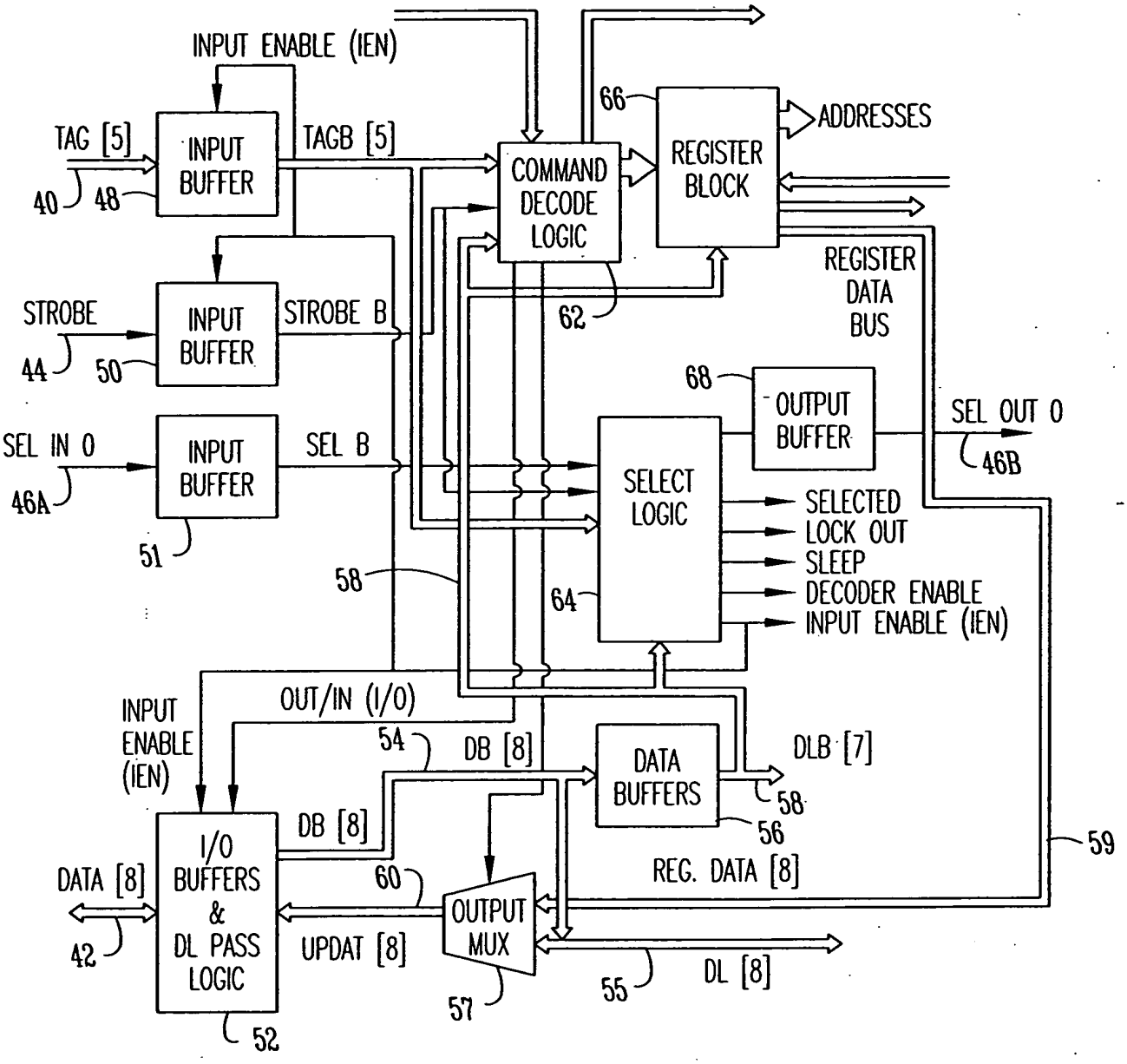
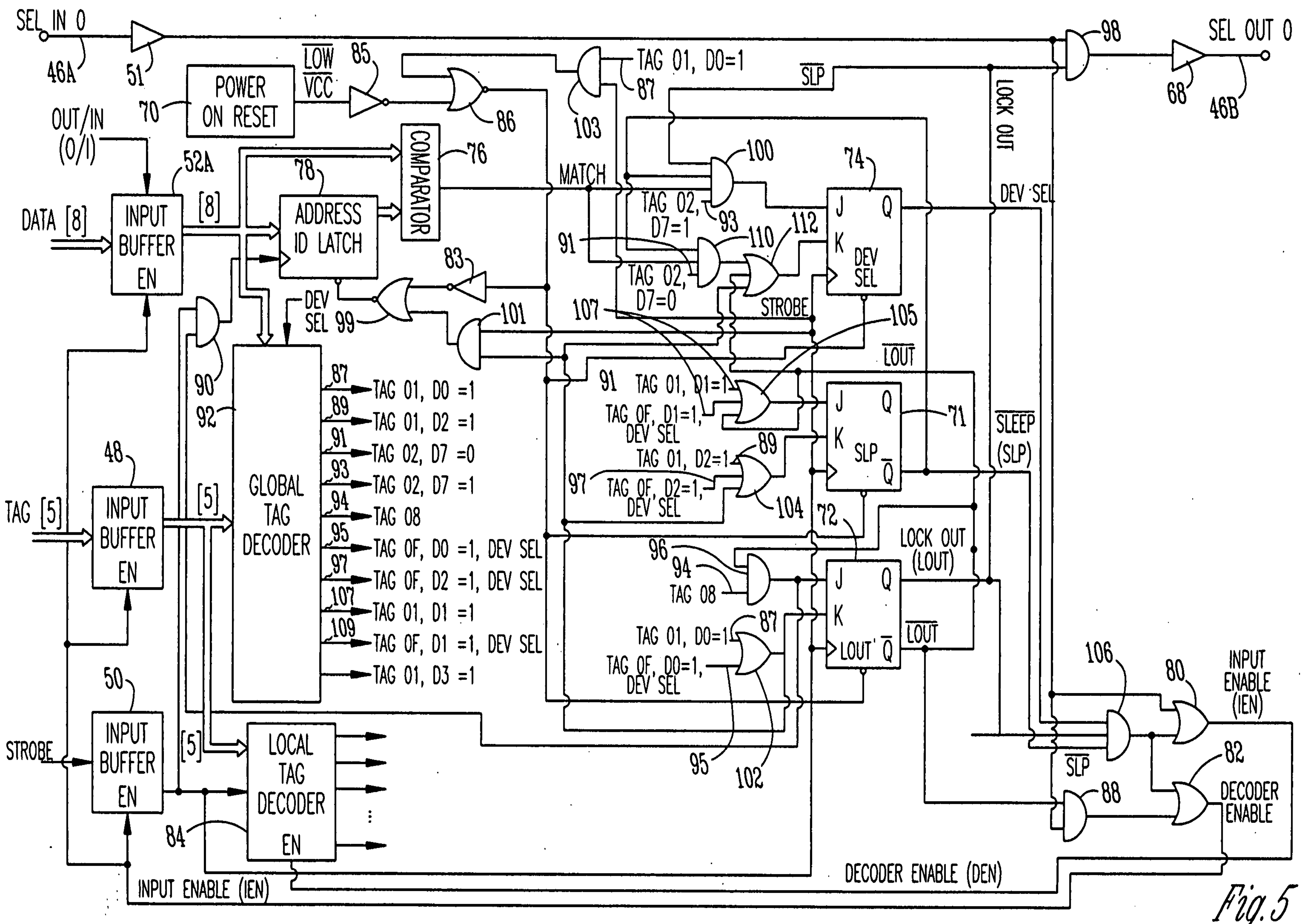

INPUT ENABLE (IEN)
TAG [5]
INPUT BUFFER
TAGB [5]
40
48
COMMAND DECODE LOGIC
66
REGISTER BLOCK
ADDRESSES
REGISTER DATA BUS
62
STROBE
INPUT BUFFER
STROBE B
44
50
68
OUTPUT BUFFER
SEL OUT 0
46B
SEL IN 0
INPUT BUFFER
SEL B
46A
51
SELECT LOGIC
SELECTED
LOCK OUT
SLEEP
DECODER ENABLE
INPUT ENABLE (IEN)
58
64
INPUT ENABLE (IEN)
OUT/IN (I/O)
54
DB [8]
DATA BUFFERS
DLB [7]
58
56
59
DB [8]
I/O BUFFERS & DL PASS LOGIC
DATA [8]
60
OUTPUT MUX
REG. DATA [8]
42
UPDAT [8]
57
55
DL [8]
52

Fig. 4


SEL IN 0
46A
51
POWER ON RESET
70
LOW VCC
85
86
OUT/IN (0/I)
52A
DATA [8]
INPUT BUFFER EN
[8]
78
ADDRESS ID LATCH
COMPARATOR
76
83
DEV SEL 99
101
90
92
GLOBAL TAG DECODER
87 TAG 01, D0 =1
89 TAG 01, D2 =1
91 TAG 02, D7 =0
93 TAG 02, D7 =1
94 TAG 08
95 TAG 0F, D0 =1, DEV SEL
97 TAG 0F, D2 =1, DEV SEL
107 TAG 01, D1 =1
109 TAG 0F, D1 =1, DEV SEL
TAG 01, D3 =1
48
TAG [5]
[5]
50
STROBE
LOCAL TAG DECODER EN
84
INPUT ENABLE (IEN)
DECODER ENABLE (DEN)
103
TAG 01, D0=1
87
MATCH
100
TAG 02, D7=1
93
91
110
112
TAG 02, D7=0
STROBE
74
J Q K DEV SEL
107
105
LOUT
91 TAG 01, D1=1
TAG 0F, D1=1, DEV SEL
89
TAG 01, D2=1
97 TAG 0F, D2=1, DEV SEL
104
71
J Q K SLP Q
72
96
94
TAG 08
TAG 01, D0=1
87
TAG 0F, D0=1, DEV SEL
95
102
J Q K LOUT Q
LOCK OUT (LOUT)
LOUT
SLP
LOCK OUT
DEV SEL
SLEEP (SLP)
98
SEL OUT 0
68
46B
106
80
INPUT ENABLE (IEN)
82
DECODER ENABLE
SLP
88
Fig. 5

SELECT LOGIC										
INPUTS							OUTPUTS (LATCHES)			
TAG BUS (HEX)	DATA BUS	$\overline{LOW\ VCC}$ ($\overline{LVCC}$)	LOCK OUT (LOUT)	DEV SEL (DSEL)	SLEEP (SLP)	MATCH	LOCK OUT (LOUT)	DEV SEL (DSEL)	SLEEP (SLP)	ADD ID LATCH
01H	D0=1	1	X	X	X	X	RESET	RESET	RESET	RESET
0FH	D0=1	1	X	1	X	X	RESET	RESET	RESET	RESET
X	X	0	X	X	X	X	RESET	RESET	RESET	RESET
08H	DEV ADD	1	0	X	X	X	SET	PREV	PREV	LOAD
01H	D1=1	1	1	X	X	X	PREV	PREV	SET	PREV
0FH	D1=1	1	1	1	X	X	PREV	PREV	SET	PREV
01H	D3=1	1	X	X	X	X	PREV	RESET	PREV	PREV
01H	D2=1	1	1	1	X	X	PREV	PREV	RESET	PREV
0FH	D2=1	1	1	1	X	X	PREV	PREV	RESET	PREV
02H	D7=1	1	1	1	0	1	PREV	SET	PREV	PREV
02H	D7=0	1	1	1	0	1	PREV	RESET	PREV	PREV

Fig. 6

ENABLE & SELECT OUT LOGIC						
INPUTS				OUTPUTS		
$\overline{\text{LOW VCC}}$ (LVCC)	LOCK OUT (LOUT)	DEV SEL (DSEL)	SLEEP (SLP)	INPUT ENABLE (IEN)	SEL OUT (SOUT)	DECODER ENABLE (DEN)
0	X	X	X	SEL IN	0	0
1	0	X	X	SEL IN	0	SEL IN
1	1	0	0	SEL IN	SEL IN	0
1	1	0	1	SEL IN	SEL IN	0
1	1	1	0	1	SEL IN	1
1	1	1	1	SEL IN	SEL IN	0

Fig. 7

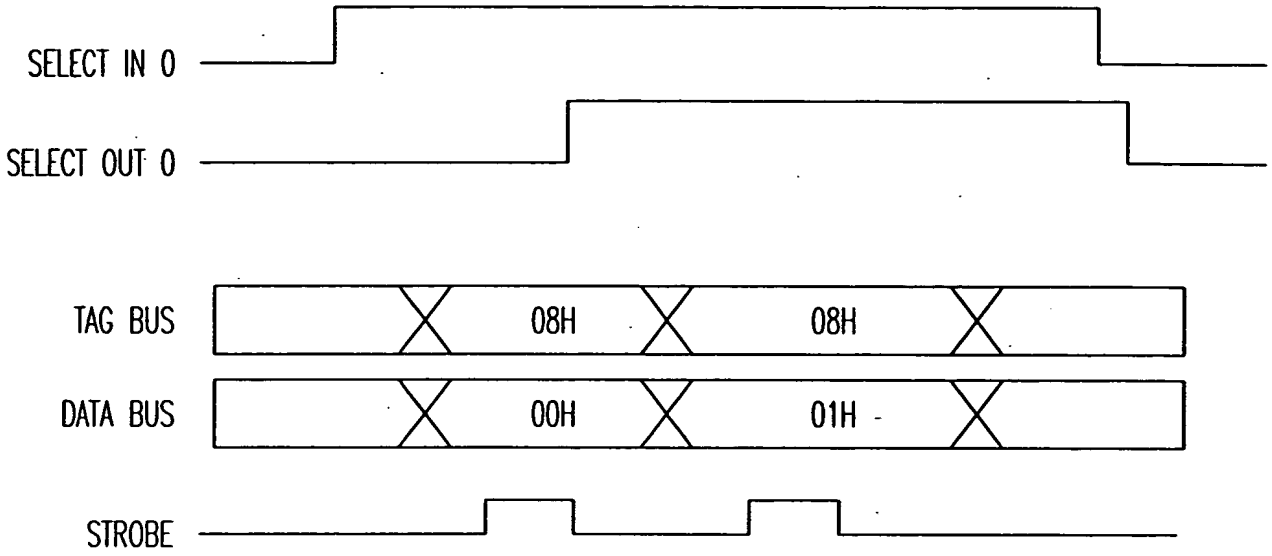

SELECT IN 0
SELECT OUT 0
TAG BUS
08H
08H
DATA BUS
00H
01H
STROBE

Fig. 8A

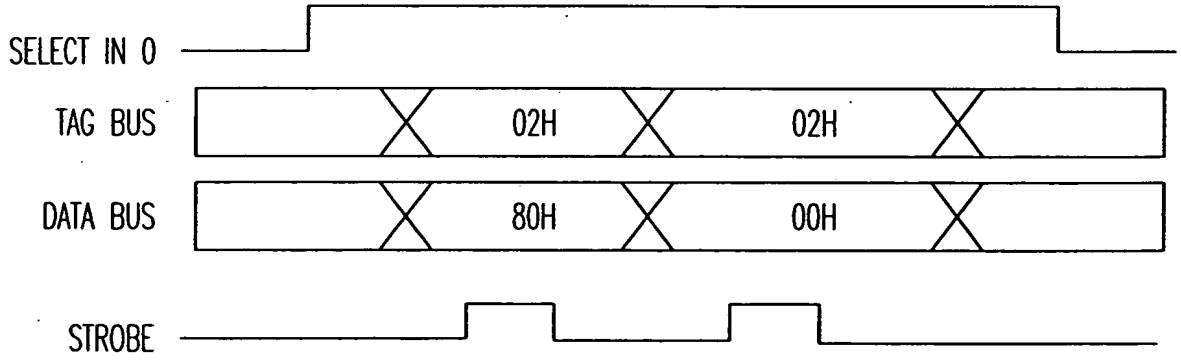

SELECT IN 0
TAG BUS
02H
02H
DATA BUS
80H
00H
STROBE

Fig. 8B

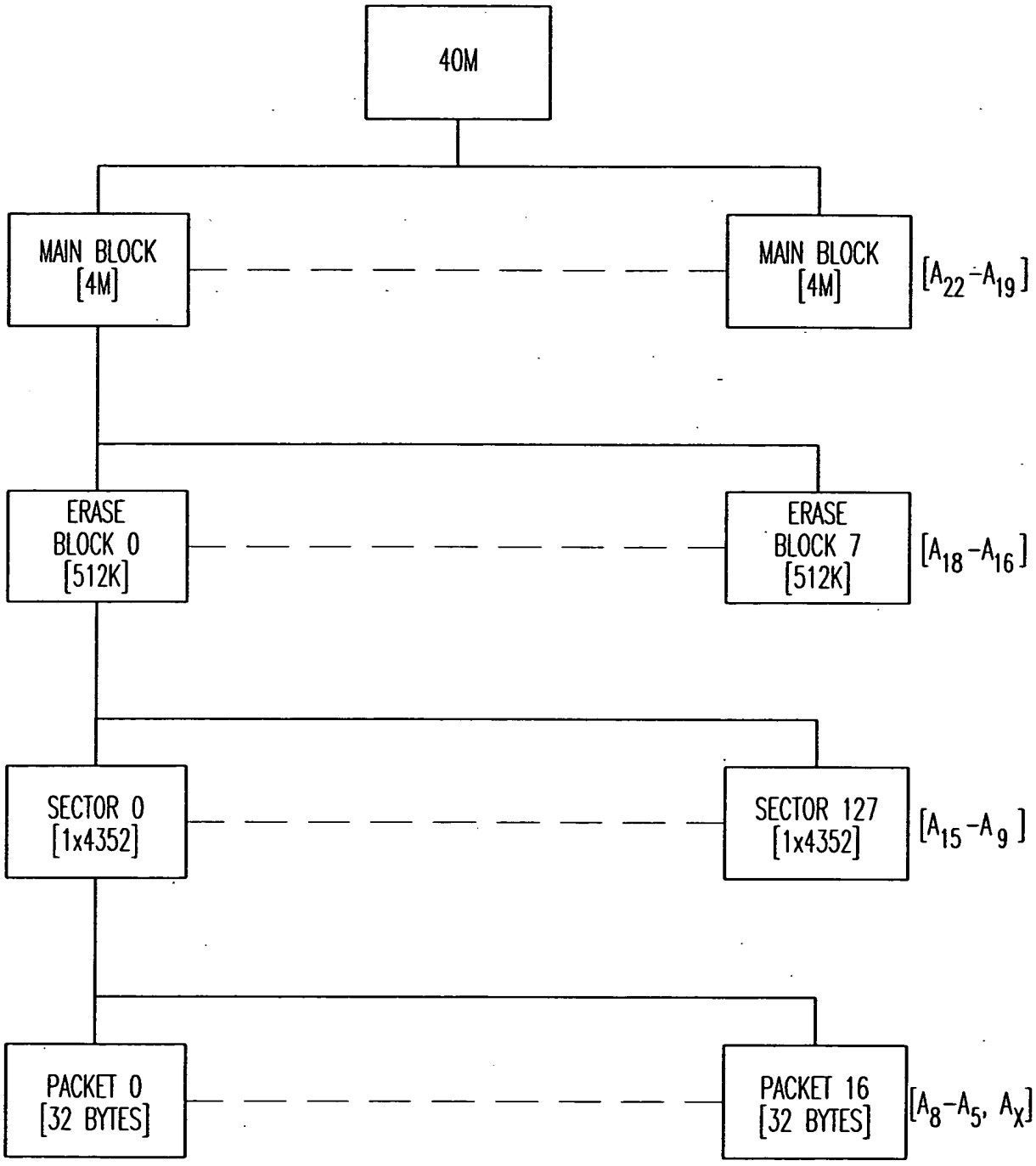

40M
MAIN BLOCK [4M]
MAIN BLOCK [4M]
[A22-A19]
ERASE BLOCK 0 [512K]
ERASE BLOCK 7 [512K]
[A18-A16]
SECTOR 0 [1x4352]
SECTOR 127 [1x4352]
[A15-A9]
PACKET 0 [32 BYTES]
PACKET 16 [32 BYTES]
[A8-A5, AX]

Fig. 9

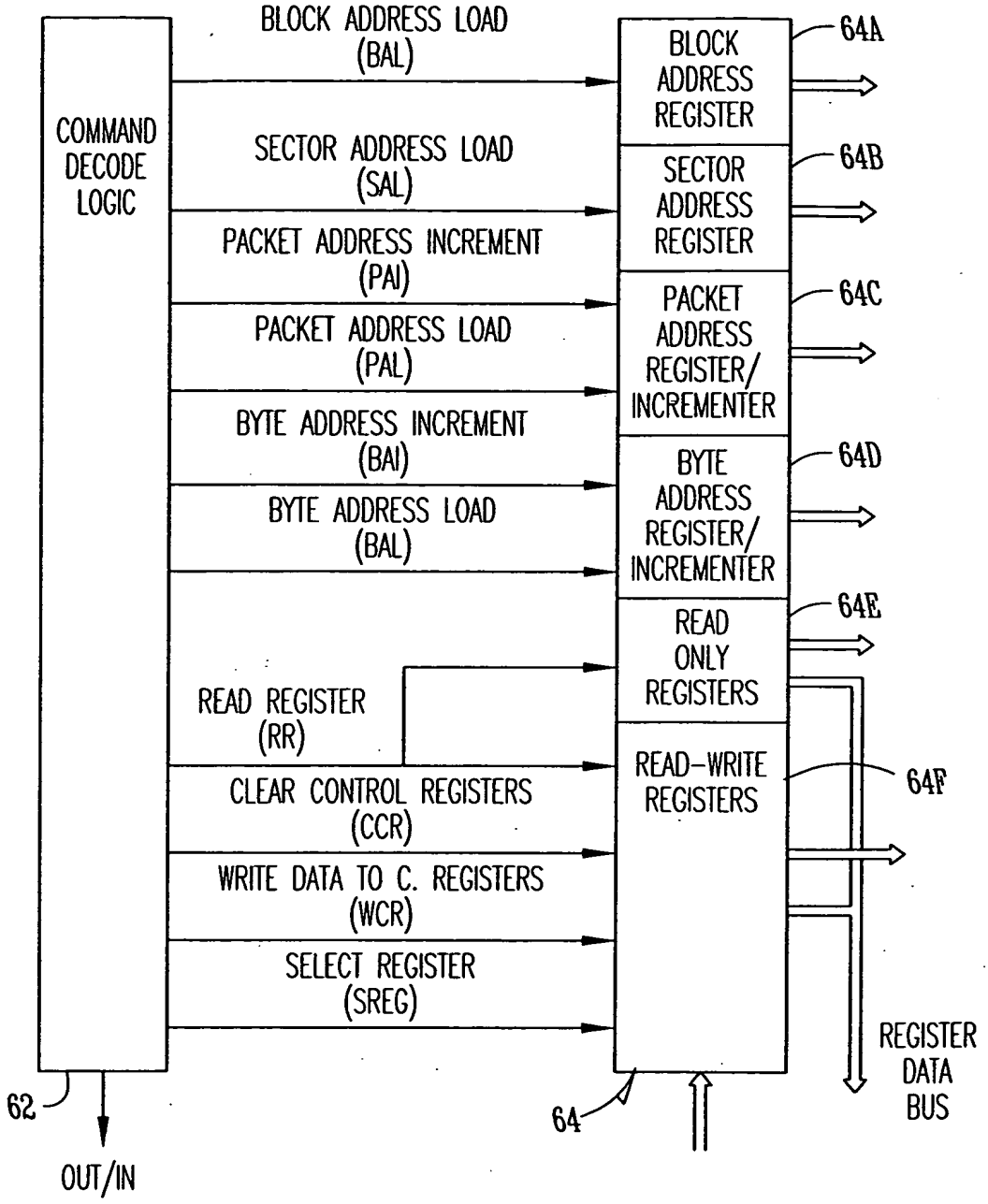

COMMAND DECODE LOGIC
BLOCK ADDRESS LOAD (BAL)
SECTOR ADDRESS LOAD (SAL)
PACKET ADDRESS INCREMENT (PAI)
PACKET ADDRESS LOAD (PAL)
BYTE ADDRESS INCREMENT (BAI)
BYTE ADDRESS LOAD (BAL)
READ REGISTER (RR)
CLEAR CONTROL REGISTERS (CCR)
WRITE DATA TO C. REGISTERS (WCR)
SELECT REGISTER (SREG)
BLOCK ADDRESS REGISTER
SECTOR ADDRESS REGISTER
PACKET ADDRESS REGISTER/ INCREMENTER
BYTE ADDRESS REGISTER/ INCREMENTER
READ ONLY REGISTERS
READ-WRITE REGISTERS
64A
64B
64C
64D
64E
64F
REGISTER DATA BUS
62
OUT/IN
64

Fig. 10

INPUTS						INPUTS																
TAG BUS (HEX)	DATA BUS	LOCK OUT	SLEEP	DEV SEL	DECODER ENABLE	BAI	BAL	BLAL	PAI	PAL	SAL	CLRADD	SREG	CCR	RCR	WREG	RDR	WDR	SAL	OUT/IN	$\overline{LVCC}$	COMMENTS
xxH	xxxxxxxx	0	x	x	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	LOW POWER
xxH	xxxxxxxx	1	1	x	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	LOW POWER
xxH	xxxxxxxx	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	1	DESELECT MODE
03H	e/dxxaaaaa	x	x	x	1	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0	1	LOAD PACKET ADDR.
04H	xaaaaaaa	x	x	x	1	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	1	LOAD SECTOR ADDR.
05H	xaaaaaaa	x	x	x	1	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0	1	LOAD BLOCK ADDR.
07H	xxxxxxxx	x	x	x	1	0	0	0	1	0	0	1	0	0	0	0	0	0	0	0	1	INCR. PACKET ADDR.
09H	e/dxxaaaaa	x	x	x	1	0	1	0	0	0	0	1	0	0	0	0	0	0	0	0	1	LOAD BYTE ADDR. SET INCR ON/OFF
0AH	dddddddd	x	x	x	1	?	0	0	0	0	0	1	0	0	0	0	0	1	0	0	1	LOAD PGM DATA REGISTERS
0BH	xxrrrrr	x	x	x	1	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	1	SELECT CONTROL REG
0CH	dddddddd	x	x	x	1	0	0	0	0	0	0	1	0	0	0	1	0	0	0	0	1	LOAD DATA TO REG
0DH	xxxxxxxx	x	x	x	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	INCREMENT BYTE REG.
0EH	xxxxxxxx	x	x	x	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	LATCH SA DATA
0FH	xx001000	x	x	x	1	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	1	CLEAR CONTROL REG.
---	xx010000	x	x	x	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	CLEAR ADDR. REG.
19H	zzzzzzzz	x	x	x	1	?	0	0	0	0	0	1	0	0	0	0	1	0	0	1	1	READ DATA
1AH	zzzzzzzz	x	x	x	1	0	0	0	0	0	0	1	0	0	1	0	0	0	0	1	1	READ CONTROL REG.

Fig. 11

REGISTER 00H	ID CODE						
[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0

Fig. 12A

REGISTER 01H	BLOCK ADDRESS						
	A_{22}	A_{21}	A_{20}	A_{19}	A_{18}	A_{17}	A_{16}
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0

Fig. 12B

REGISTER 02H	SECTOR ADDRESS REGISTER						
	A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0

Fig. 12C

REGISTER 03H		PACKET ADDRESS REGISTER					
PACKET INCREMENT ENABLE/ DISABLE			A_X	A_8	A_7	A_6	A_5
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0

Fig. 12D

REGISTER 04H		BYTE ADDRESS REGISTER					
BYTE INCREMENT ENABLE/ DISABLE		A_4	A_3	A_2	A_1	A_0	
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0

Fig. 12E

REGISTER 05H		CONTROL A					
			REF VOLTAGE GENERATOR ENABLE				
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0

Fig. 12F

REGISTER 06H		CONTROL B					
WORD LINE TRIM [7]	WORD LINE TRIM [6]	WORD LINE TRIM [5]	WORD LINE TRIM [4]	WORD LINE TRIM [3]	WORD LINE TRIM [2]	WORD LINE TRIM [1]	WORD LINE TRIM [0]
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0

Fig. 12G

REGISTER 07H		CONTROL C					
ENABLE LOW CURRENT PUMP	CONNECT PROGRAM VOLTAGE TO BIT LINE (PGM)	ENABLE WORD LINE SWITCH					
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0

Fig. 12H

REGISTER 08H		CONTROL D					
ENABLE S.A. REFERENCE GENERATOR	BIT LINE TRIM (READ) [1]	BIT LINE TRIM (READ) [0]		SENSE MARGIN TRIM (READ) [3]	SENSE MARGIN TRIM (READ) [2]	SENSE MARGIN TRIM (READ) [1]	SENSE MARGIN TRIM (READ) [0]
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0

Fig. 12I

REGISTER 09H	CONTROL E						
			SELECT ALL WORD LINES	$\overline{D}$ESELCT ALL WORD LINES	SELECT ALL MAIN BLOCKS	SELECT ALL ERASE BLOCKS	$\overline{D}$ESELCT ALL MAIN LINES
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0

Fig. 12J

REGISTER 0AH	CONTROL F						
CONNECT DL BUS TO DZ BUS						DISCHARGE BIT LINES	$\overline{F}$LOAT BIT LINES
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0

Fig. 12K

REGISTER 0BH	CONTROL G						
	BYPASS PROGRAM LATCHES		ENABLE SENSE CIRCUITS				
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0

Fig. 12L

REGISTER 0CH		CONTROL H					
		BIT LINE TRIM PROGRAM [2]	BIT LINE TRIM PROGRAM [1]	BIT LINE TRIM PROGRAM [0]	ENABLE BL SWITCH	ENABLE HIGH CURRENT PUMP	
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0

Fig. 12M

REGISTER 0DH		CONTROL I					
	ENABLE NEGATIVE PUMPS	SOURCE LINE TRIM (ERASE) [2]	SOURCE LINE TRIM (ERASE) [1]	SOURCE LINE TRIM (ERASE) [0]	ENABLE SOURCE SWITCH CIRCUIT	WORD LINE SUPPLY	
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0

Fig. 12N

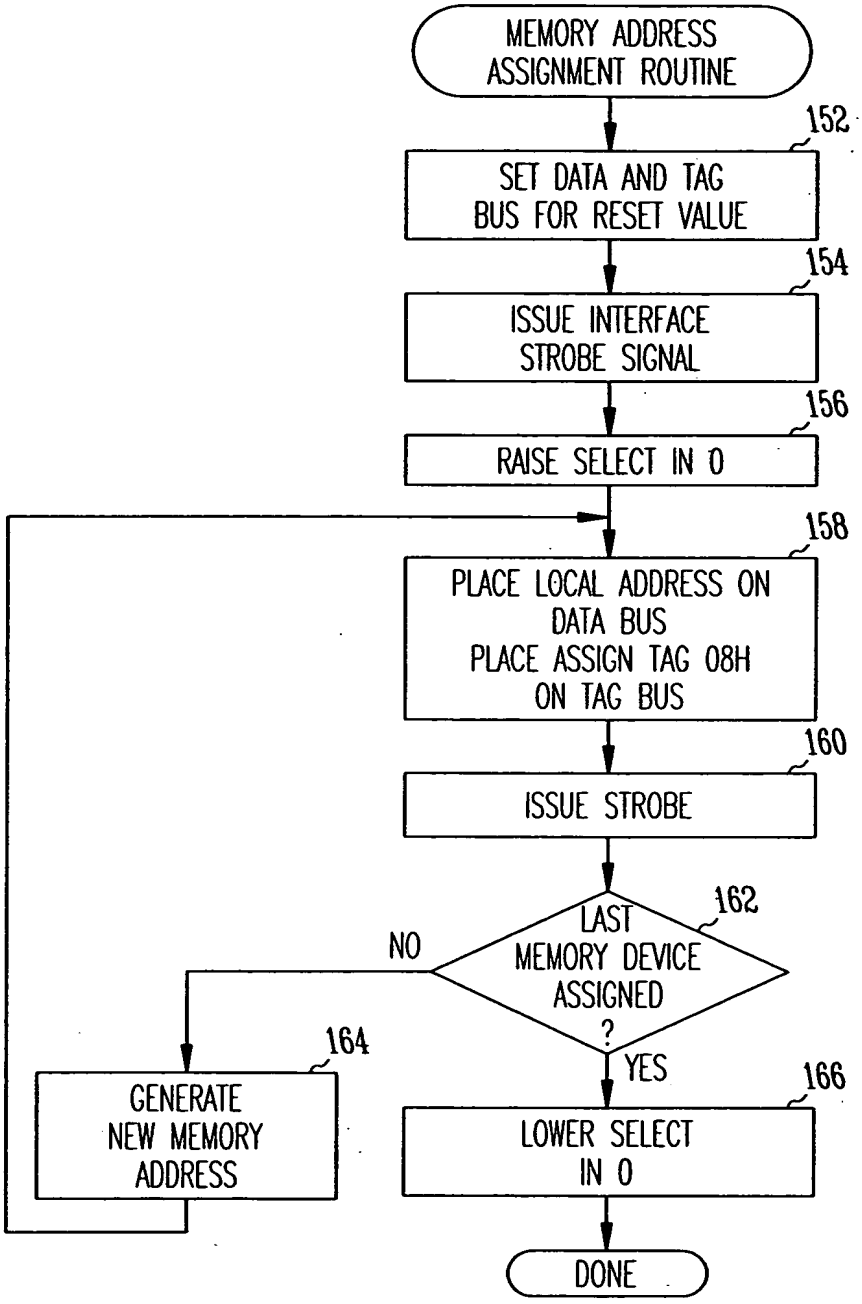

MEMORY ADDRESS ASSIGNMENT ROUTINE
152
SET DATA AND TAG BUS FOR RESET VALUE
154
ISSUE INTERFACE STROBE SIGNAL
156
RAISE SELECT IN 0
158
PLACE LOCAL ADDRESS ON DATA BUS
PLACE ASSIGN TAG 08H ON TAG BUS
160
ISSUE STROBE
162
LAST MEMORY DEVICE ASSIGNED ?
NO
YES
164
GENERATE NEW MEMORY ADDRESS
166
LOWER SELECT IN 0
DONE

Fig. 13

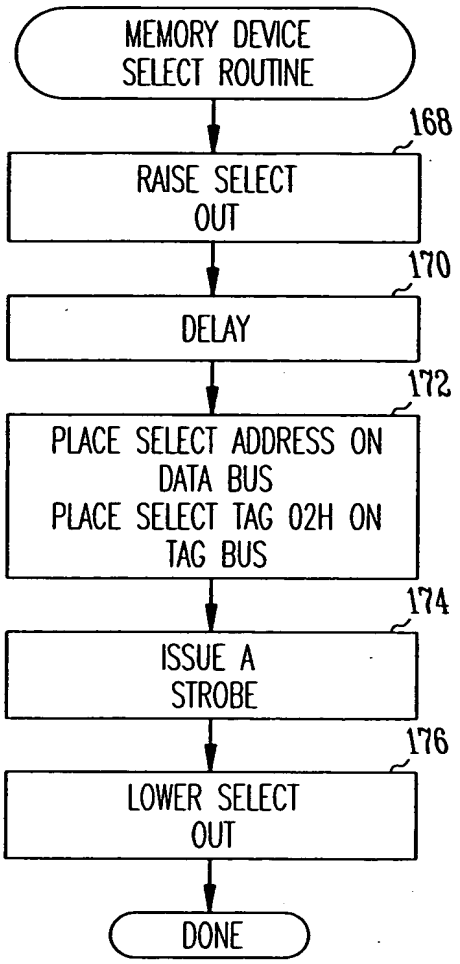

MEMORY DEVICE SELECT ROUTINE
168
RAISE SELECT OUT
170
DELAY
172
PLACE SELECT ADDRESS ON DATA BUS
PLACE SELECT TAG 02H ON TAG BUS
174
ISSUE A STROBE
176
LOWER SELECT OUT
DONE

Fig. 14

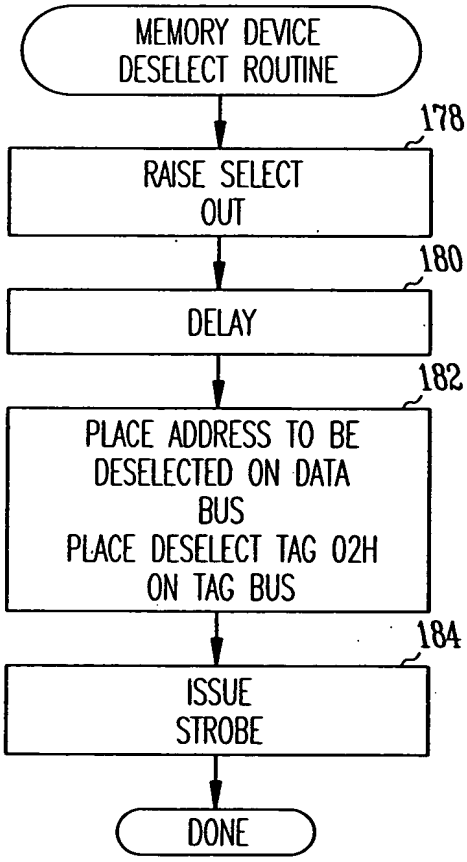

MEMORY DEVICE DESELECT ROUTINE
178
RAISE SELECT OUT
180
DELAY
182
PLACE ADDRESS TO BE DESELECTED ON DATA BUS
PLACE DESELECT TAG 02H ON TAG BUS
184
ISSUE STROBE
DONE

Fig. 15

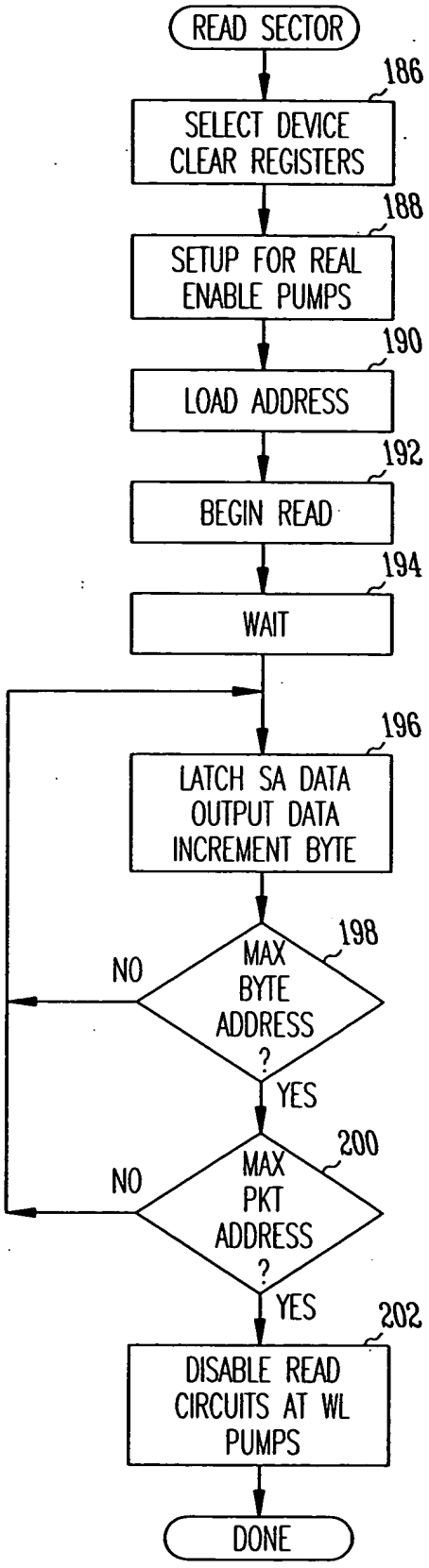

READ SECTOR
186
SELECT DEVICE
CLEAR REGISTERS
188
SETUP FOR REAL
ENABLE PUMPS
190
LOAD ADDRESS
192
BEGIN READ
194
WAIT
196
LATCH SA DATA
OUTPUT DATA
INCREMENT BYTE
198
MAX
BYTE
ADDRESS
?
NO
YES
200
MAX
PKT
ADDRESS
?
NO
YES
202
DISABLE READ
CIRCUITS AT WL
PUMPS
DONE

Fig. 16

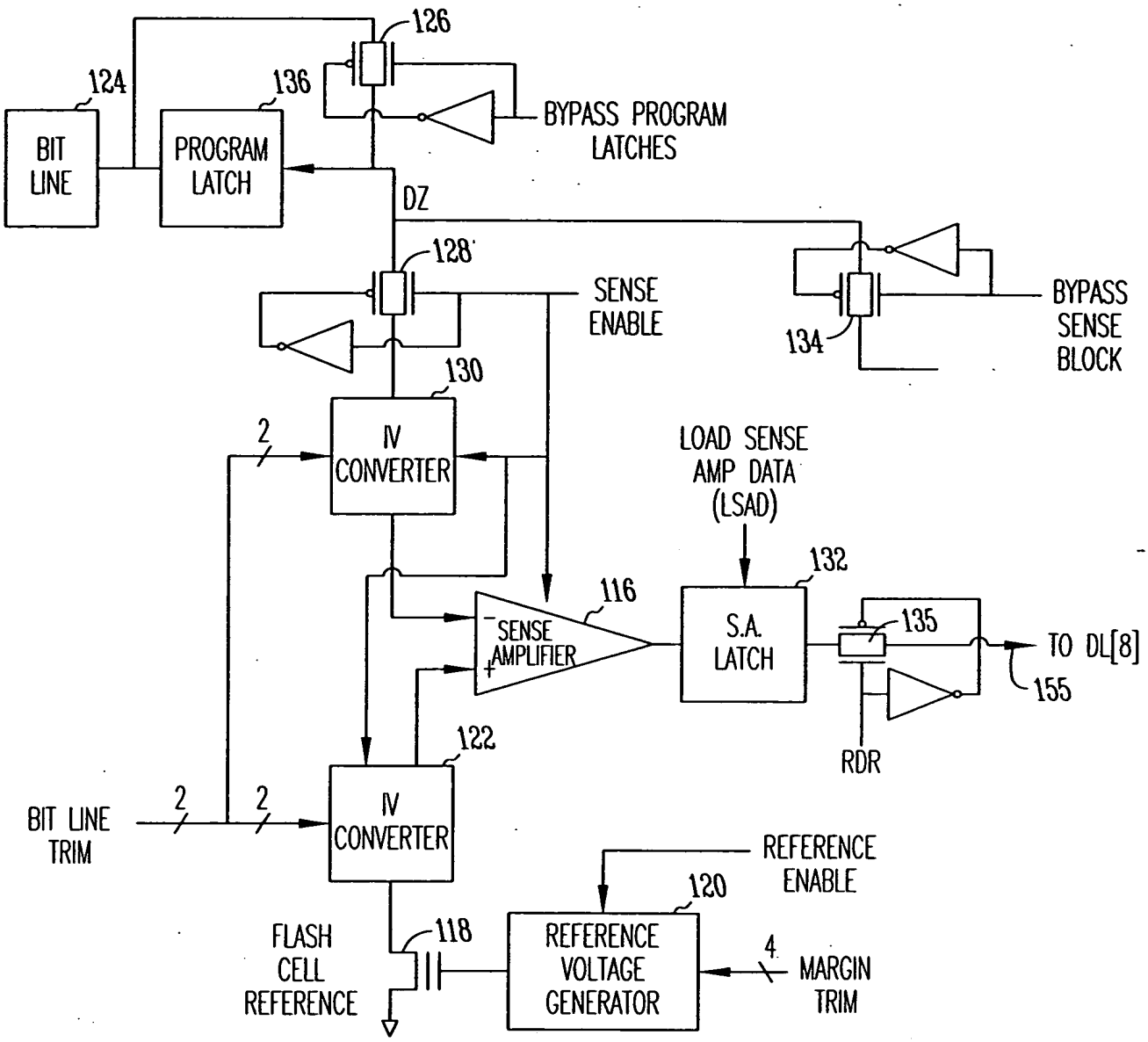

126
124
136
BIT LINE
PROGRAM LATCH
BYPASS PROGRAM LATCHES
DZ
128
SENSE ENABLE
134
BYPASS SENSE BLOCK
130
2
IV CONVERTER
LOAD SENSE AMP DATA (LSAD)
132
116
SENSE AMPLIFIER
S.A. LATCH
135
TO DL[8]
155
RDR
122
BIT LINE TRIM
2
2
IV CONVERTER
REFERENCE ENABLE
120
FLASH CELL REFERENCE
118
REFERENCE VOLTAGE GENERATOR
4
MARGIN TRIM

Fig. 17

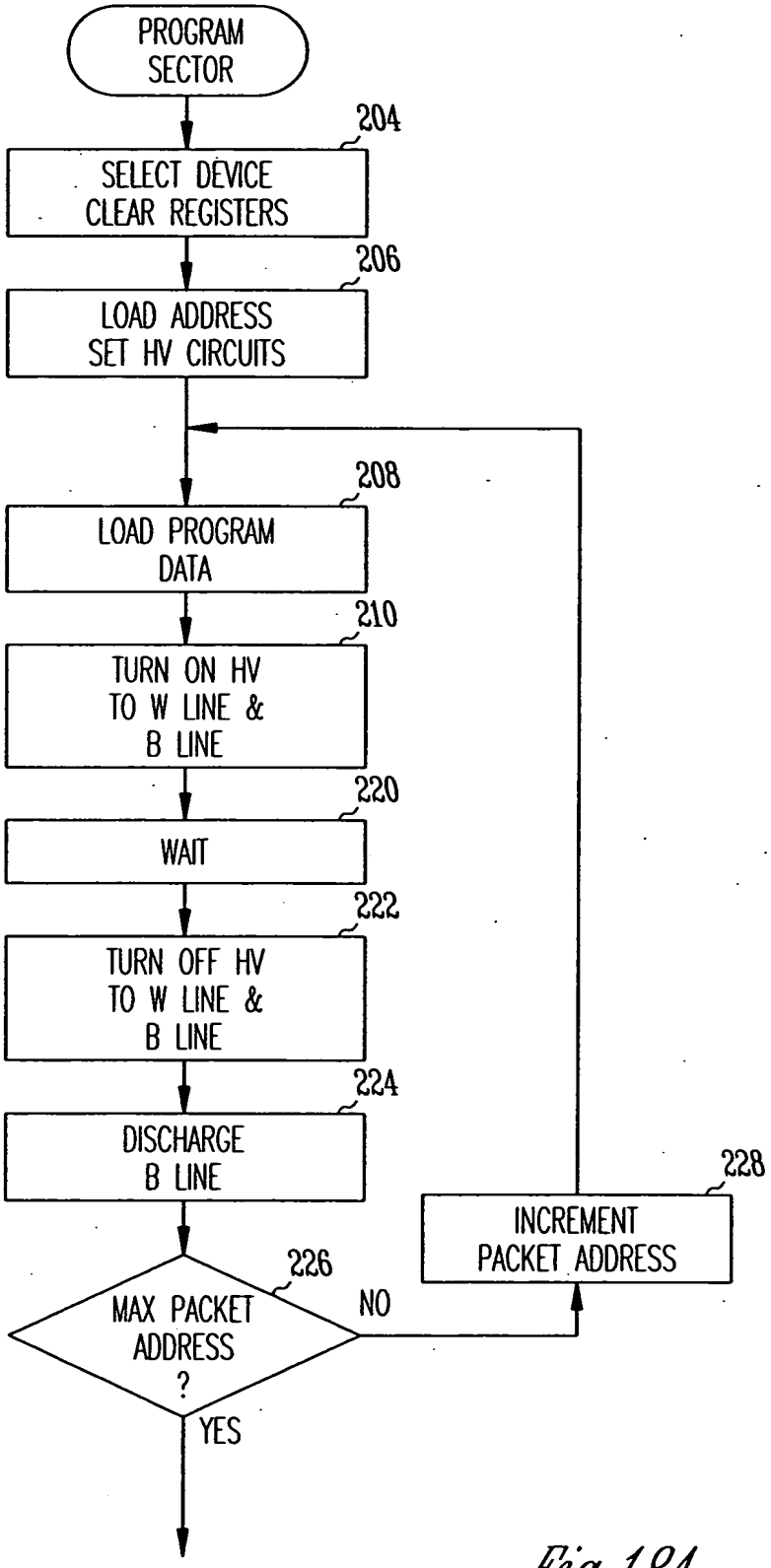

PROGRAM SECTOR
204
SELECT DEVICE CLEAR REGISTERS
206
LOAD ADDRESS SET HV CIRCUITS
208
LOAD PROGRAM DATA
210
TURN ON HV TO W LINE & B LINE
220
WAIT
222
TURN OFF HV TO W LINE & B LINE
224
DISCHARGE B LINE
226
MAX PACKET ADDRESS ?
NO
228
INCREMENT PACKET ADDRESS
YES
(Fig.18B)

Fig. 18A

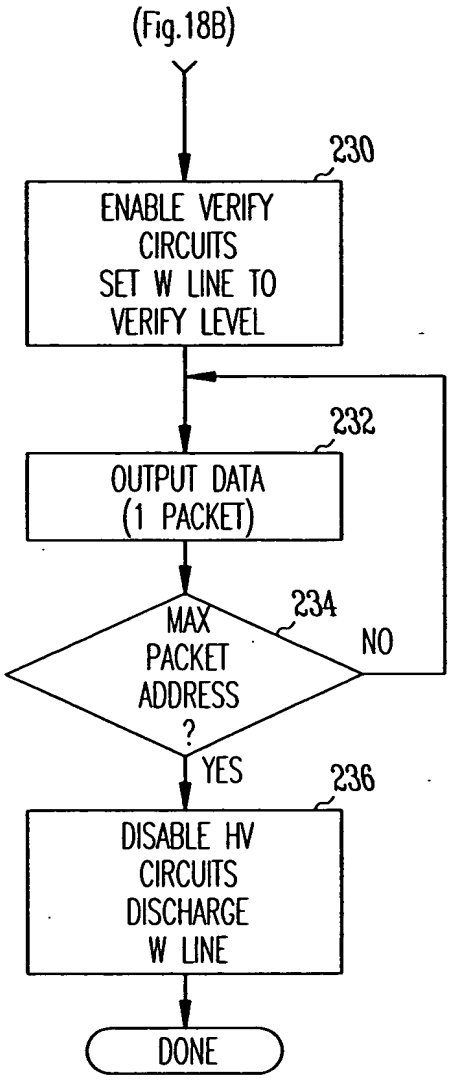

(Fig.18B)
230
ENABLE VERIFY CIRCUITS SET W LINE TO VERIFY LEVEL
232
OUTPUT DATA (1 PACKET)
234
MAX PACKET ADDRESS ?
NO
YES
236
DISABLE HV CIRCUITS DISCHARGE W LINE
DONE

Fig. 18B

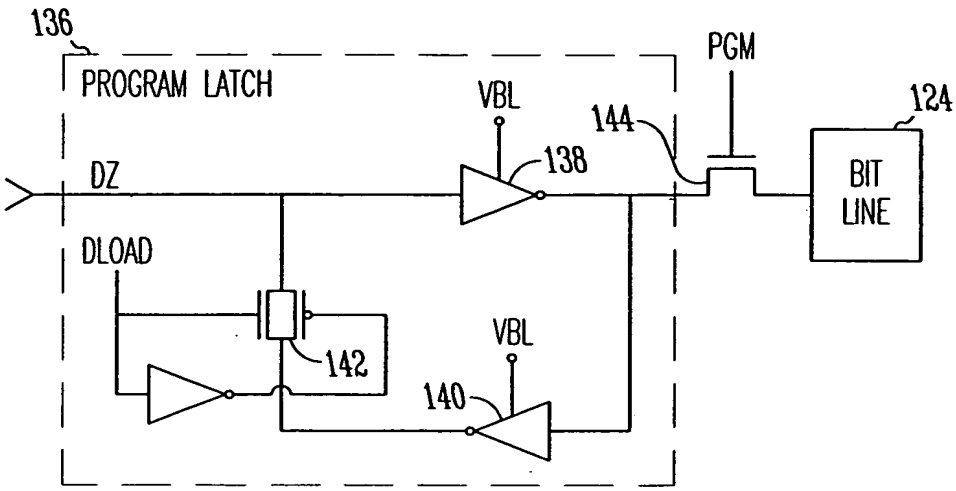

136
PROGRAM LATCH
PGM
VBL
124
144
138
DZ
BIT
LINE
DLOAD
142
VBL
140

Fig. 19

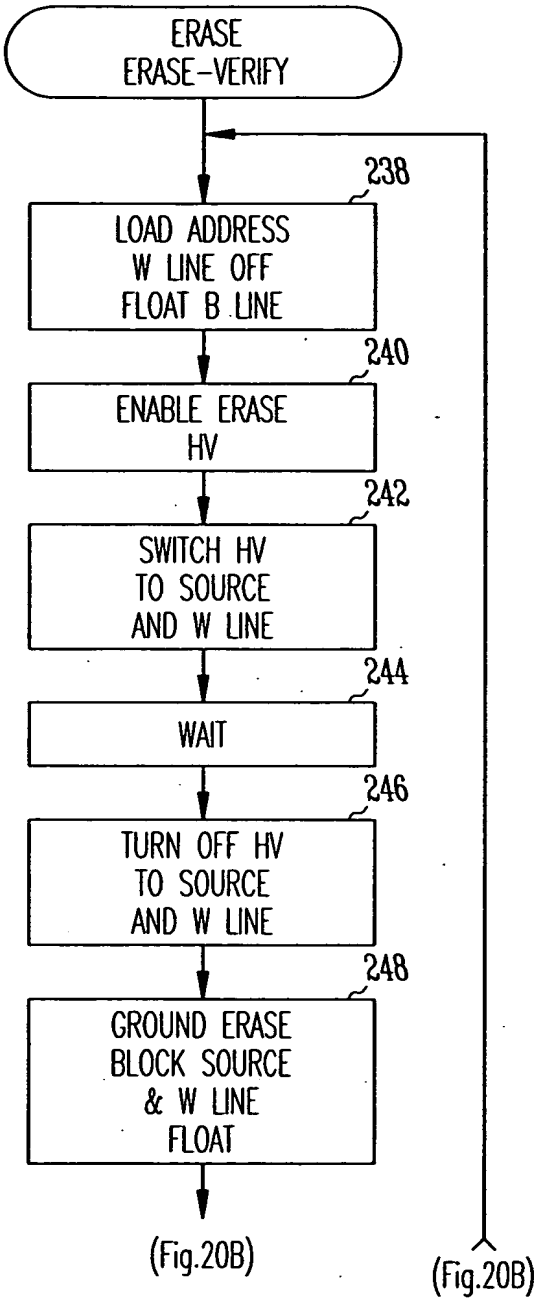

ERASE
ERASE-VERIFY
238
LOAD ADDRESS
W LINE OFF
FLOAT B LINE
240
ENABLE ERASE
HV
242
SWITCH HV
TO SOURCE
AND W LINE
244
WAIT
246
TURN OFF HV
TO SOURCE
AND W LINE
248
GROUND ERASE
BLOCK SOURCE
& W LINE
FLOAT
(Fig.20B)
(Fig.20B)

Fig.20A

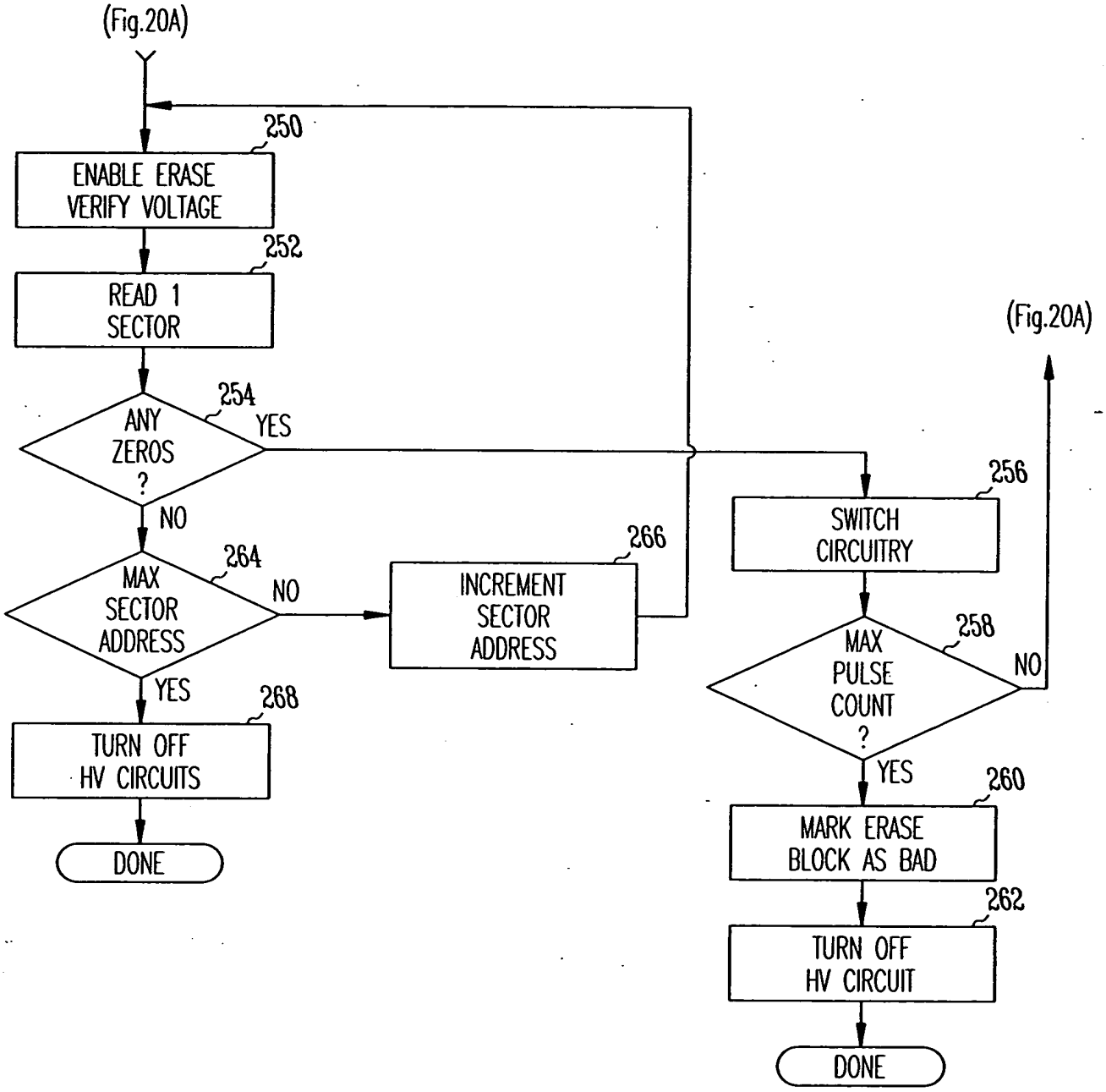

(Fig.20A)
250
ENABLE ERASE VERIFY VOLTAGE
252
READ 1 SECTOR
254
ANY ZEROS ?
YES
NO
264
MAX SECTOR ADDRESS
NO
266
INCREMENT SECTOR ADDRESS
YES
268
TURN OFF HV CIRCUITS
DONE
(Fig.20A)
256
SWITCH CIRCUITRY
258
MAX PULSE COUNT ?
NO
YES
260
MARK ERASE BLOCK AS BAD
262
TURN OFF HV CIRCUIT
DONE

Fig.20B

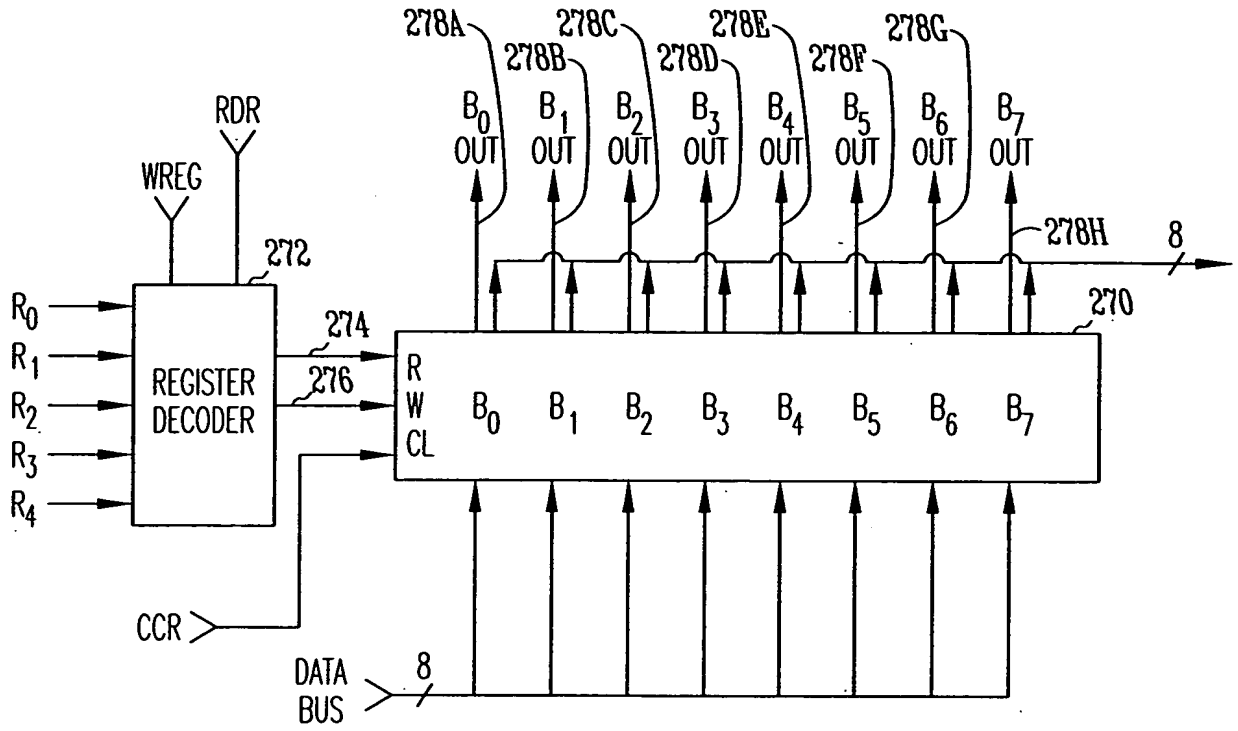

278A
278B
278C
278D
278E
278F
278G
278H
B_0 OUT
B_1 OUT
B_2 OUT
B_3 OUT
B_4 OUT
B_5 OUT
B_6 OUT
B_7 OUT
8
270
RDR
WREG
272
R_0
R_1
R_2
R_3
R_4
REGISTER DECODER
274
276
R
W
CL
B_0 B_1 B_2 B_3 B_4 B_5 B_6 B_7
CCR
DATA BUS
8

Fig.21

Sheet 9 of 26

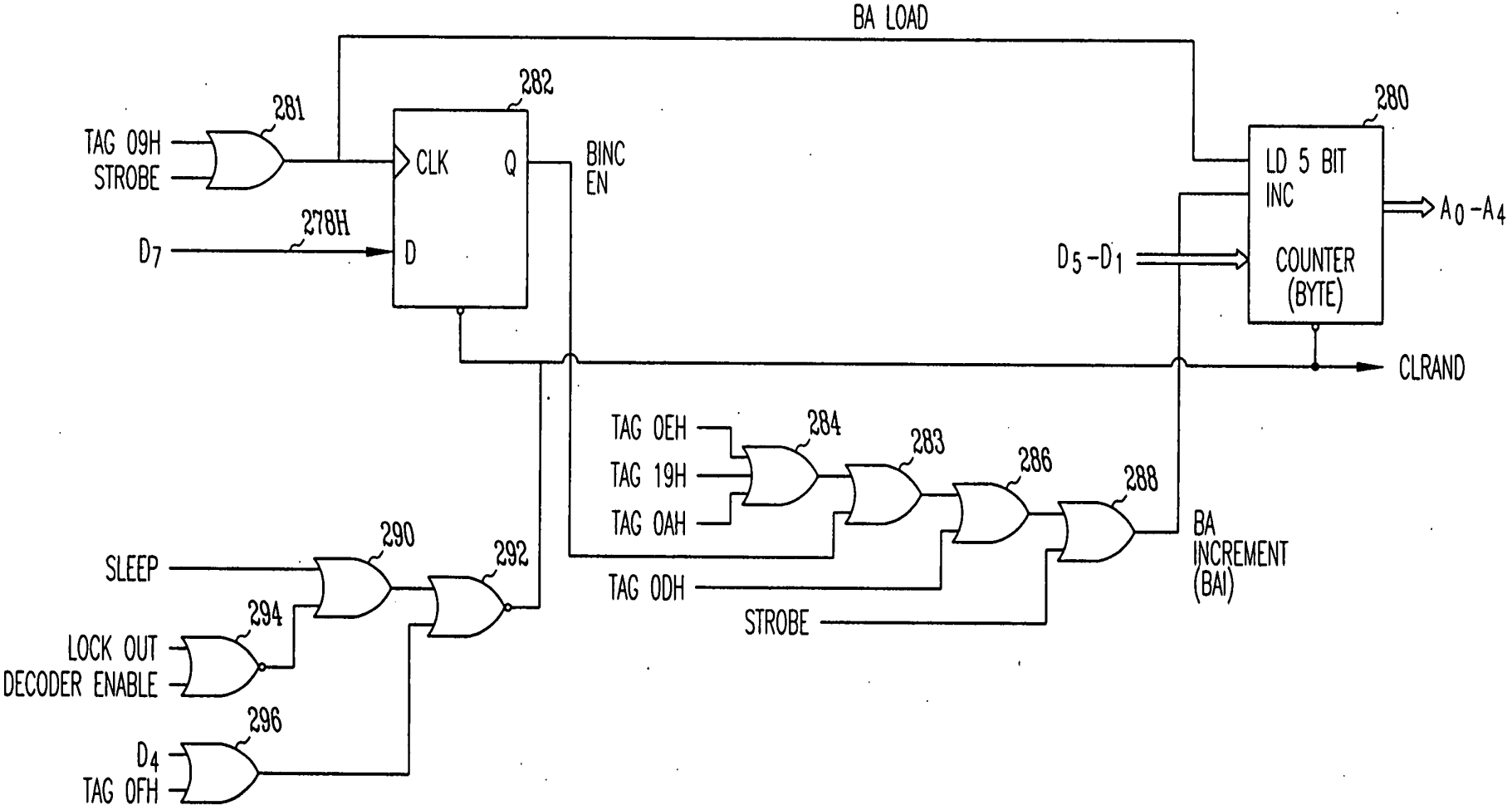


Fig.22

UNITED STATES

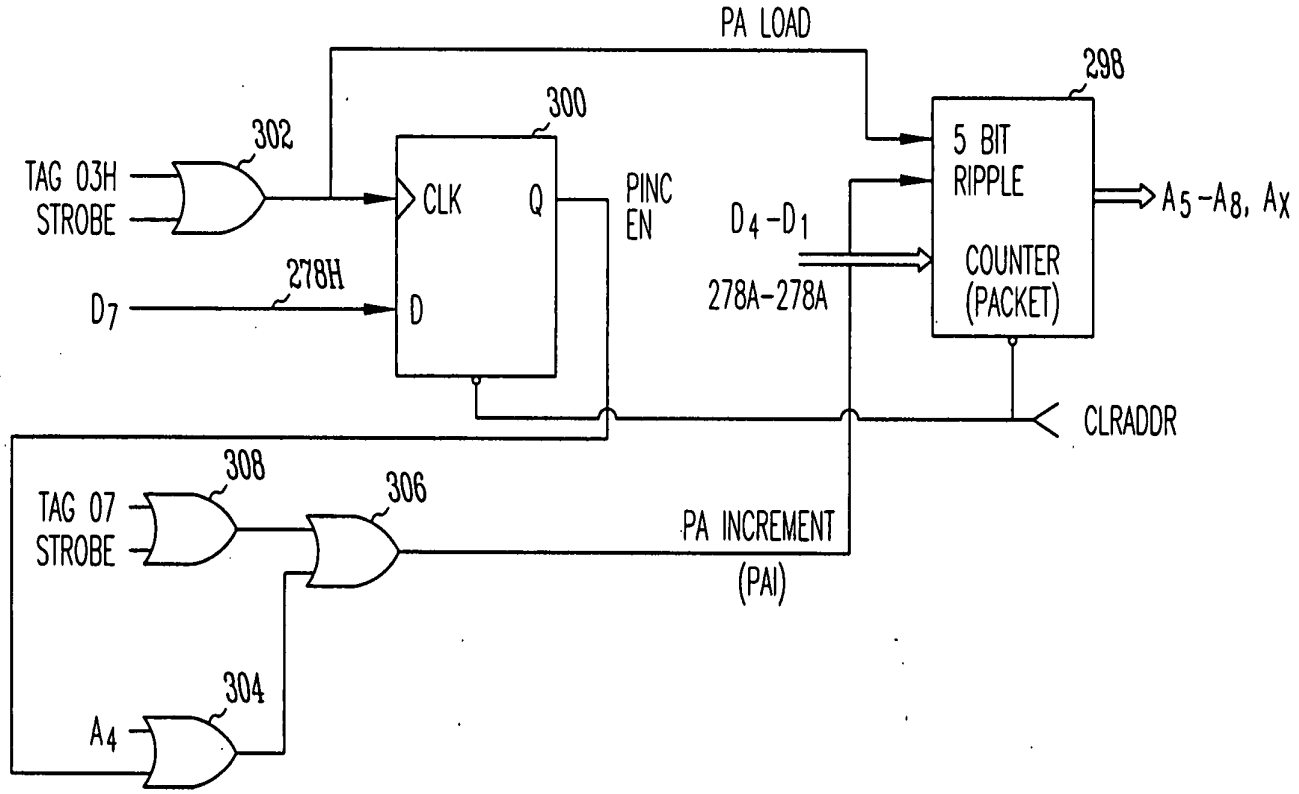


Fig.23

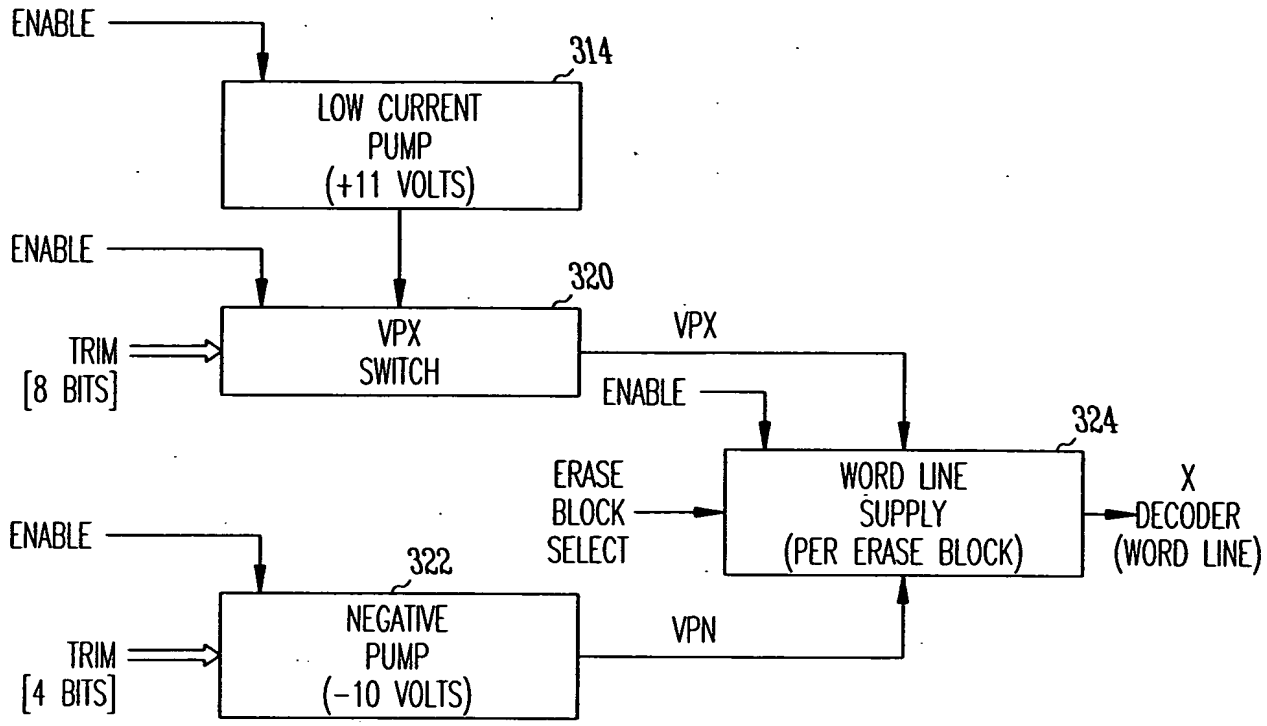


Fig.24A

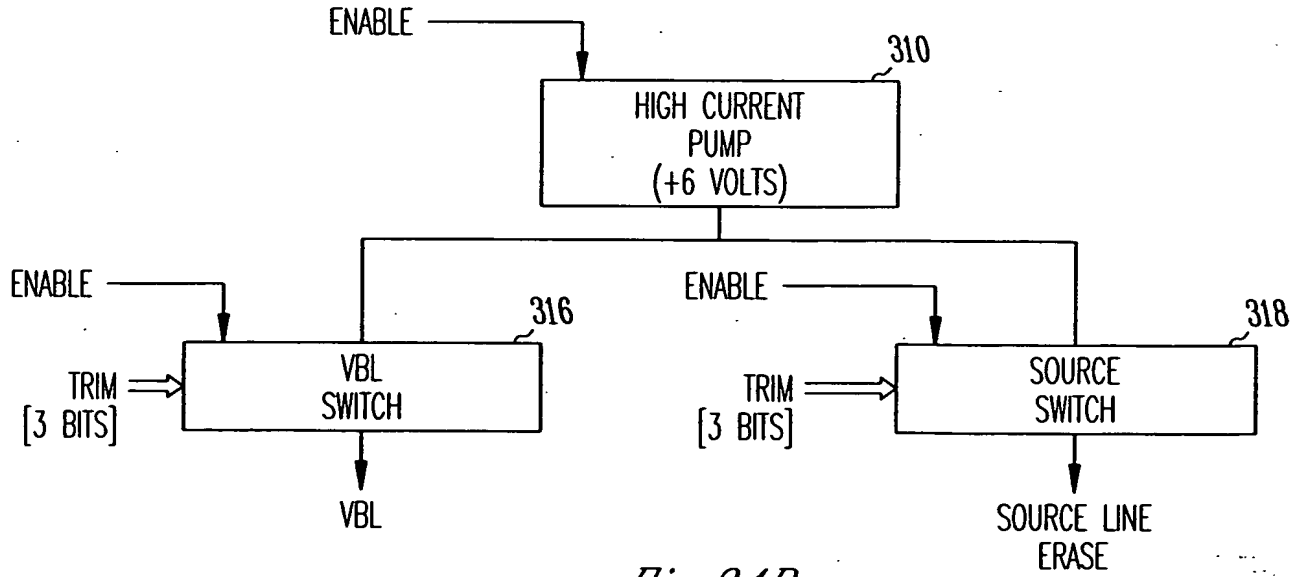


Fig.24B

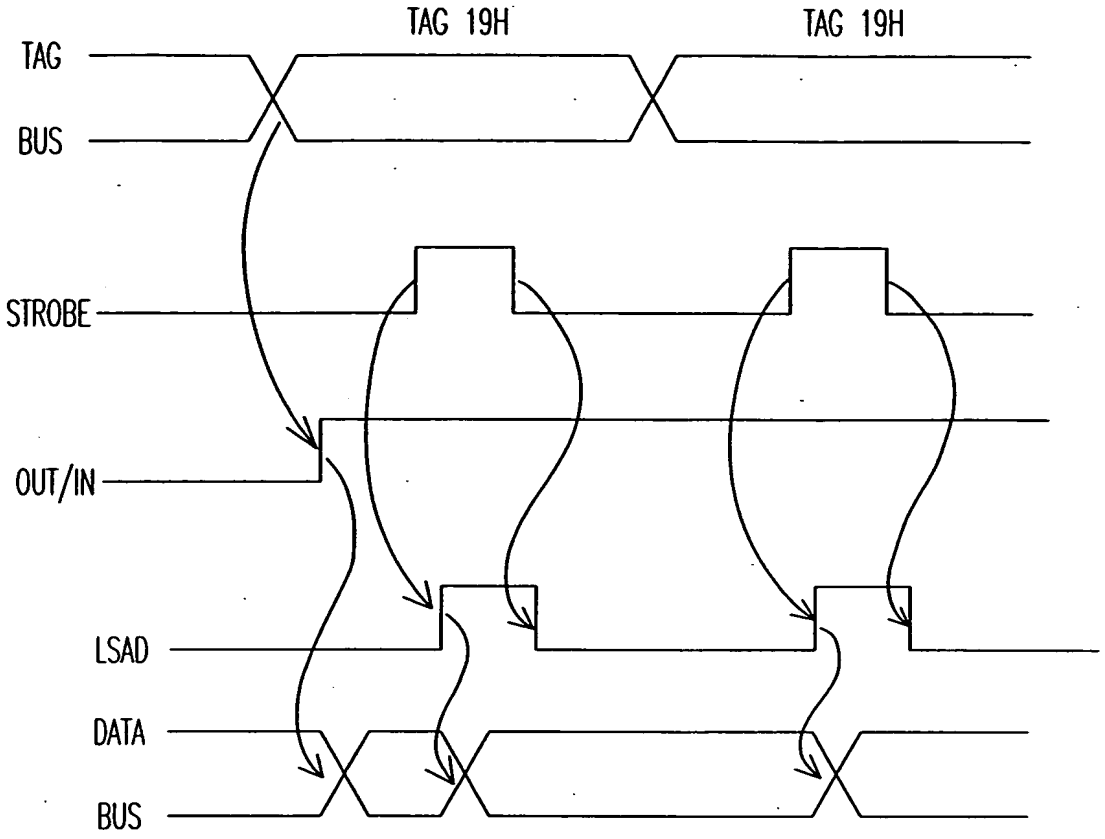


Fig.25

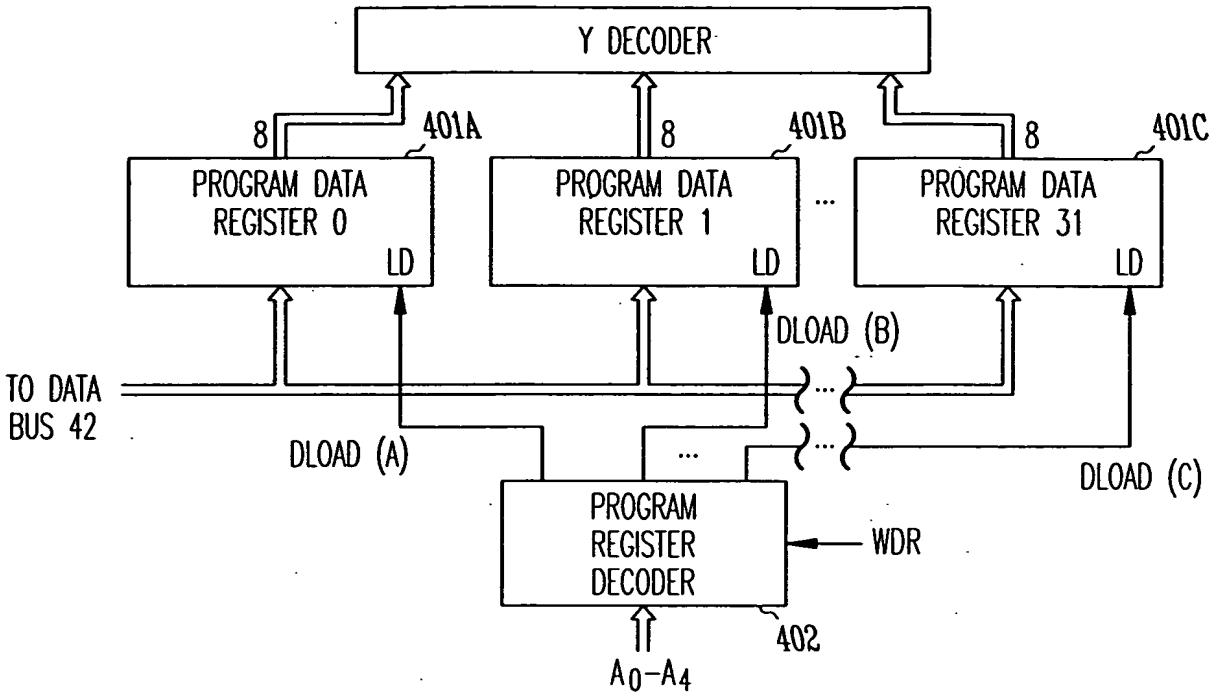

Y DECODER
8
401A
8
401B
8
401C
PROGRAM DATA REGISTER 0
LD
PROGRAM DATA REGISTER 1
LD
PROGRAM DATA REGISTER 31
LD
DLOAD (B)
TO DATA BUS 42
DLOAD (A)
DLOAD (C)
PROGRAM REGISTER DECODER
WDR
402
A0-A4

Fig. 26